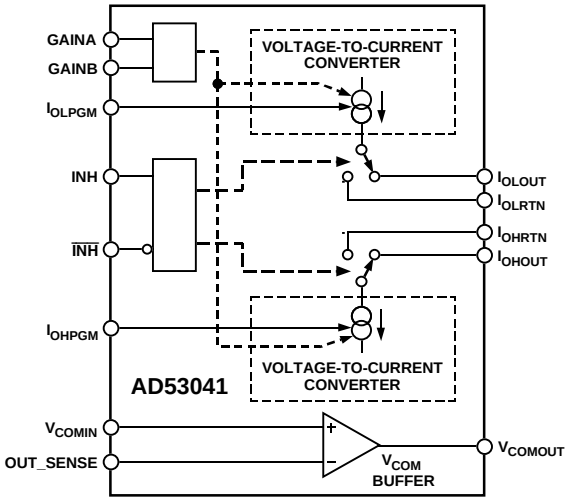
High Speed Active Load with Inhibit Mode

AD53041

FEATURES
±50 mA Voltage Programmable Current Range
Three Selectable Gain Ranges
1.7 ns Propagation Delay
Inhibit Mode Function
High Speed Differential Inputs for Maximum Flexibility
Ultrasmall 20-Lead PSOP Package with Built-In Heatsink

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems

FUNCTIONAL BLOCK DIAGRAM



GAINA	GAINB	FULL-SCALE CURRENT
0	0	50mA
0	1	16mA
1	0	5mA
1	1	NOT VALID

PRODUCT DESCRIPTION

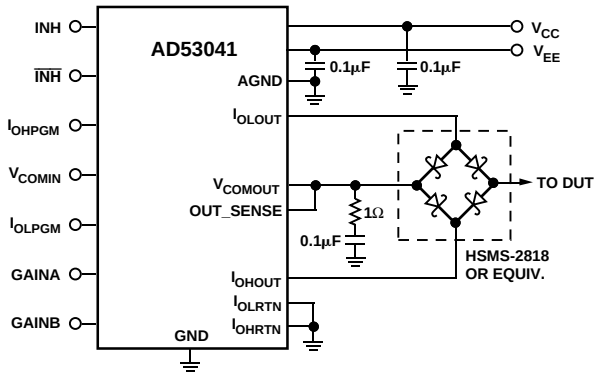
The AD53041 is a complete, high speed, current switching load designed for use in linear, digital or mixed signal test systems. Combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities in an ultrasmall 20-lead, PSOP package with a built-in heatsink.

Featuring current programmability of up to ±50 mA, the AD53041 is designed to force the device under test to source or sink the programmed I_{OH} and I_{OL} currents. I_{OH} and I_{OL} currents are determined by applying a corresponding voltage (5 V = 50 mA, 16 mA, 5 mA) to the I_{OHPGM} and I_{OLPGM} pins. The voltage-to-current conversion is performed within the AD53041, thus allowing the current levels to be set by a standard voltage out digital-to-analog converter.

The AD53041 transition from I_{OH} to I_{OL} occurs when the output voltage of the device under test slews above or below the programmed threshold or commutation voltage. The commutation voltage is programmable from –2 V to +7 V, covering the large spectrum of logic devices while able to support the large current specifications (48 mA) typically associated with line drivers. To test I/O devices, the active load can be switched into a high impedance state (Inhibit Mode), electrically removing the active load from the path through the Inhibit Mode feature. The active load leakage current in Inhibit is typically 100 nA.

The Inhibit input circuitry is implemented using high speed differential inputs with a common-mode voltage range of –2 V to +3 V and a maximum differential voltage of 3 V. This allows for direct interface to precision differential ECL timing or the simplicity of switching active load from a single ended TTL or CMOS logic source. With switching speeds from I_{OH} or I_{OL} into Inhibit of less than 2.0 ns, the AD53041 can be electrically removed from the signal path "on the fly."

The AD53041 is available in a 20-lead, PSOP package with a built-in-heatsink and is specified to operate over the ambient commercial temperature range from –25°C to +85°C.



NOT SHOWN: THE AGND PINS ARE THE HIGH QUALITY GROUND REFERENCE FOR THE VOLTAGE-TO-CURRENT CONVERTERS. THE GND PINS PROVIDE RETURN PATHS FOR INTERNAL CURRENTS. V_{CC} IS THE POSITIVE SUPPLY, V_{EE} IS THE NEGATIVE SUPPLY. ALL GROUND PINS SHOULD BE CONNECTED TO THE SYSTEM ANALOG GROUND PLANE.

Figure 1. Typical Application Circuit

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD53041–SPECIFICATIONS

(All specifications apply at T_J = +85°C ± 5°C. $+V_S$ = +10.5 V ± 3%, $-V_S$ = –5.2 V ± 3% unless otherwise specified. V_{COMOUT} is bypassed to ground with a series RC consisting of a 1 Ω resistor and a 0.1 μF capacitor, and is also connected directly to OUT_SENSE. All temperature coefficients are characterized over T_J = 75°C–95°C.)

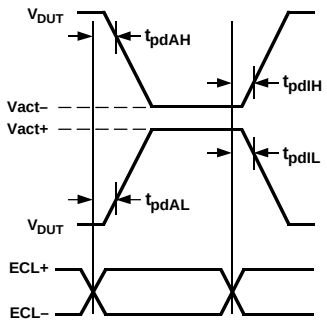
Parameter	Min	Typ	Max	Units	Test Conditions
INPUT CHARACTERISTICS					
INH, $\overline{INH}$					
Input Voltage	–2	ECL	0	V	
Bias Current	–1		1	mA	INH, $\overline{INH}$ = –2 V, 0 V
GAINA, GAINB					
Input Voltage	0	TTL/CMOS	5	V	
Bias Current	0		2	mA	GAINA, GAINB = 5 V
I_{OHPGM}, I_{OLPGM} Voltage Range					
I_{OH}, 0 to + Full Scale, Any Gain Range	–0.1		5.2	V	$V(I_{OHOUT})$ = –2 V, 7 V
I_{OL}, 0 to – Full Scale, Any Gain Range	–0.1		5.2	V	$V(I_{OLOUT})$ = –2 V, 7 V
I_{OHPGM}, I_{OLPGM} Bias Current	–300		300	μA	$V(I_{OHPGM})$ = +5 V, $V(I_{OLPGM})$ = 0 V
V_{COM} BUFFER					
Voltage Range	–2		7	V	±50 mA Output Current
Offset		±5		mV	V_{COM} = 0 V
Offset Drift		0.1		mV/°C	V_{COM} = 0 V
Nonlinearity		±5		mV	V_{COM} = –2 V to 7 V
Input Bias Current	–50		50	μA	V_{COM} = –2 V to 7 V
Output Resistance		<1		Ω	V_{COM} = 0 V, I_{OUT} = ±50 mA
OUTPUT CHARACTERISTICS					
Full-Scale Current Range					See Functional Block Diagram
Range 0		50		mA	
Range 1		16		mA	
Range 2		5		mA	
Offset Error					$V(I_{OHPGM})$ = $V(I_{OLPGM})$ = 100 mV,
Range 0	–1		1	mA	$V(I_{OHOUT})$ = ±2 V, $V(I_{OLOUT})$ = ±2 V
Range 1	–0.3		0.3	mA	
Range 2	–0.3		0.3	mA	
Offset Drift					$V(I_{OHPGM})$ = $V(I_{OLPGM})$ = 100 mV,
Range 0		1		μA/°C	$V(I_{OHOUT})$ = $V(I_{OLOUT})$ = 0 V
Range 1		1		μA/°C	
Range 2		1		μA/°C	
Gain Error					
Range 0		<1		% FSR	
Range 1		<5		% FSR	
Range 2		<8		% FSR	
Gain Drift					
Range 0		1		μA/°C	
Range 1		0.5		μA/°C	
Range 2		0.3		μA/°C	
Gain Ratio Drift					
Range 1 to Range 0		0.01		%/°C	
Range 2 to Range 0		0.01		%/°C	
Nonlinearity		±0.05		% FSR	Range 0
Common-Mode Error		±0.05		%FSR	Range 0
PSRR		±0.1		%FSR/V	Range 0, $V(I_{OHPGM})$ = $V(I_{OLPGM})$ = 100 mV, Either Supply Over Operating Range
OUTPUT VOLTAGE RANGE					
I_{OHOUT}, I_{OHRTN}	–2.5		7.5	V	I_{OH} = 50 mA
I_{OLOUT}, I_{OLRTN}	–2.5		7.5	V	I_{OL} = 50 mA

Parameter	Min	Typ	Max	Units	Test Conditions
LEAKAGE CURRENTS					Range 0, Bridge Diode Leakage Not Included
I_{OH} Inhibit-Mode Leakage	–1		1	µA	$V(I_{OHOUT})$ = –2.5 V to 7.5 V, Inhibited
I_{OL} Inhibit-Mode Leakage	–1		1	µA	$V(I_{OLOUT})$ = –2.5 V to 7.5 V, Inhibited
I_{OH} Off-State Leakage	–3		3	µA	$V(I_{OHOUT})$ = –2.5 V to 7.5 V, $V(I_{OHPGM})$ = –0.2 V
I_{OL} Off-State Leakage	–3		3	µA	$V(I_{OLOUT})$ = –2.5 V to 7.5 V, $V(I_{OLPGM})$ = –0.2 V
DYNAMIC PERFORMANCE					
Propagation Delays					
$\pm I_{MAX}$ to Inhibit		1.4		ns	Range 0, I_{MAX}, R_{LOAD} = 50 Ω
Part-to-Part Skew		1		ns	
Inhibit to $\pm I_{MAX}$		1.9		ns	Range 0, I_{MAX}, R_{LOAD} = 50 Ω
Part-to-Part Skew		1		ns	
Propagation Delay Drift		10		ps/°C	$\pm I_{MAX}$ to Inhibit, Inhibit to $\pm I_{MAX}$
Capacitance		3		pF	I_{OHOUT} or I_{OLOUT} Without Diodes
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range	15.2	15.7	16.2	V	
Positive Supply Range	10.2	10.5	10.8	V	
Negative Supply Range	–5.4	–5.2	–5.0	V	
Positive Supply Current			160	mA	Range 0, $V(I_{OHPGM})$ = $V(I_{OLPGM})$ = 5.0 V, Active
	10		60	mA	Range 0, $V(I_{OHPGM})$ = $V(I_{OLPGM})$ = 200 mV, Active
Negative Supply Current			160	mA	Range 0, $V(I_{OHPGM})$ = $V(I_{OLPGM})$ = 5.0 V, Active
	10		60	mA	Range 0, $V(I_{OHPGM})$ = $V(I_{OLPGM})$ = 200 mV, Active
Power Dissipation		2.1	2.3	W	I_{OH} = 50 mA, I_{OL} = –50 mA, Active, $V(I_{OHOUT})$ = 7 V, $V(I_{OLOUT})$ = –2 V

NOTES
Typical values are not tested or guaranteed.
Specifications subject to change without notice.

Table I. Active Load Truth Table
(Including External Diode Bridge per Figure 1; Scale Factors per Functional Block Diagram)

V(DUT)	INH	$\overline{INH}$	OUTPUT STATES (IFS Is Full-Scale Current Set by GAINA, GAINB) I_{OH}	I_{OL}	I(VDUT)
< V_{COM}	0	1	$[V(I_{OHPGM}) \div 5\ V] \times IFS$	$[V(I_{OLPGM}) \div 5\ V] \times IFS$	I_{OL}
> V_{COM}	0	1	$[V(I_{OHPGM}) \div 5\ V] \times IFS$	$[V(I_{OLPGM}) \div 5\ V] \times IFS$	I_{OH}
X	1	0	0	0	0



PROPAGATION DELAY LOAD AND TEST CONDITIONS

PARAMETER	DESCRIPTION	I_{OL}	I_{OH}	V_{DUT}	MEASURE POINT
t_{pdAH}	I_{OL} Inh → Act	50mA	50mA	0V	0.50V
t_{pdIL}	I_{OL} Act → Inh	50mA	50mA	0V	2.00V
t_{pdAH}	I_{OH} Inh → Act	50mA	50mA	5V	4.50V
t_{pdIH}	I_{OH} Act → Inh	50mA	50mA	5V	3.00V

Figure 2. Inhibit Propagation Delay Measurement

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . . +12 V
- $-V_S$ to GND . . . . . –7 V
- $+V_S$ to $-V_S$ . . . . . +17 V
- GND to AGND . . . . . ±0.4 V

Inputs
- INH, $\overline{INH}$ . . . . . +6 V, –3 V
- INH to $\overline{INH}$ . . . . . ±3 V
- GAINA, GAINB . . . . . +6 V, –3 V
- GAINA to GAINB . . . . . ±5 V
- V_{COMIN} . . . . . +8 V, –3 V
- I_{OHPGM}, I_{OLPGM} . . . . . +6 V, –1 V

Outputs
- I_{OHOUT}, I_{OHRTN} . . . . . +9 V, –2.5 V
- I_{OLOUT}, I_{OLRTN} . . . . . +8 V, –3.5 V
- V_{COMOUT} Short Circuit Duration . . . . . Not Protected[2]

Environmental
- Operating Temperature (Junction) . . . . . +175°C
- Storage Temperature . . . . . –65°C to +150°C
- Lead Temperature (Soldering, 10 sec)[3] . . . . . +260°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

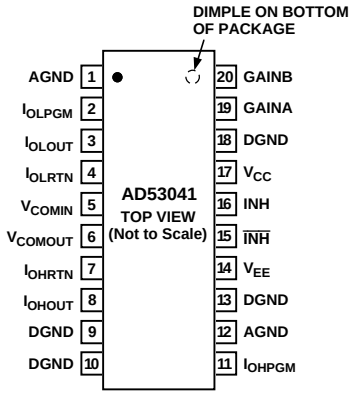
[2] Short circuit to ground or to either supply will result in the destruction of the device.

[3] To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ± 5°C (75°F ± 10°F) with relative humidity not to exceed 65%.

ORDERING GUIDE

Model	Package Description	Shipment Method, Quantity per Shipping Container	Package Option
AD53041KRP	20-Lead Power SOIC	Tube, 38 Pieces	RP-20

PIN CONFIGURATION



NOTES:
AGND IS THE HIGH-QUALITY GROUND REFERENCE FOR I_{OLPGM} AND I_{OHPGM}.
DGND IS THE SUPPLY GROUND.

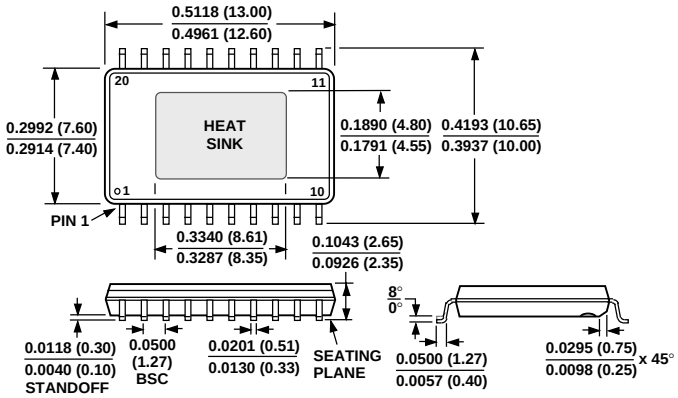
PACKAGE THERMAL CHARACTERISTICS

Air Flow, FM	θ_{JC}, °C/W	θ_{JA}, °C/W
0	4	50
50	4	49
400	4	34

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Thermally Enhanced Power Small Outline Package (PSOP) (RP-20)



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53041 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

C3004a–0–11/98

PRINTED IN U.S.A.